A CMOS 650 MHz Seventh-order Current-Mode 0.05° Equiripple Linear Phase Filter

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Abstract: **Read/write channels for hard disk drives (HDD) require high-frequency continuous time filters (CTF) [1-5]. A 650 MHz current-mode seventh-order 0.05° equiripple linear phase low-pass filter for computer hard disk read/write channels with data rates up to 1Gbit/s is presented in this paper. It is implemented in CMOS using a leap-frog multiple loop feedback structure. The operational transconductance amplifier (OTA) used is based on a differential pair and uses source degeneration to achieve linearization and tuning. Simulated using a standard 0.18μm CMOS process, the dynamic range at 1% THD of the filter is 48dB, cut-off frequency can be tuned from 590MHz to 690MHz, group delay ripple is about 5%, and power consumption is 370mW from supply voltage of 2.5V.**

I. INTRODUCTION

Read/write channels for hard disk drives (HDD) require high-frequency continuous time filters (CTF). Currently, the HDD industry is continually developing disk drives with higher data transfer rates, requiring filters with high cut-off frequencies and simultaneously achieving small group delay variation and low noise, together with improved power efficiency. As an approximate rule, for data rates up to 1 Gb/s, a filter with a cut-off frequency of at least 600MHz in the UHF frequency range is required. For technological and economic reasons, pure CMOS digital IC technologies are currently overwhelmingly favoured for both digital and analogue design. However, designing filters operating at very high frequencies in pure CMOS processes is a major challenge, because CMOS devices have a low current driving capability, which is a drawback for high speed applications.

The filter structure and design methods play an important role in the overall performance of OTA-C filters. Different architectures can result in significant performance differences for implementation of a given filter response. Design methods for high-order active filters including the cascade, LC ladder simulation, and multiple loop feedback (MLF) are well established [1-8]. The main drawback of the cascade realization is high sensitivity to filter parameter variations and component tolerances. LC ladder derived OTA-C filters have received considerable attention mainly due to the fact that they have the same low sensitivity as their original passive LC prototypes, but non-imaginary-zeros in the response cannot be realized. MLF active filters are attractive in the sense that they have low sensitivity compared to cascade topologies, and they can realize arbitrary transmission zeros. Compared to the cascade and ladder simulation methods, MLF OTA-C topologies require fewer OTAs in certain realizations of filter functions. MLF OTA-C structures offer reduced parasitic effects and simplify IC implementation, as they use only grounded capacitors. The ability to realize arbitrary zeros with these filters makes them suitable for adaptive equalization applications. Note that MLF active filters have an intrinsic drawback in that their global feedback loops introduce hard-to-minimize phase errors, which severely affect the filter frequency responses. Therefore, it is a challenging task to design an OTA suitable for a UHF MLF filter.

None of the proposed linear phase lowpass filters in the literature are based on current-mode structures. Theoretically, current-mode filters can achieve higher cut-off frequency than their voltage-mode counterparts. This paper presents a current-mode seventh-order 0.05° equiripple linear phase lowpass filter design, including a gain-boost function.

The paper is organized as follows: The OTA architecture is described in Section II. In Section III, the filter structure and synthesis is given. Simulation results and conclusions are given in Sections IV and V respectively.

II. OTA DESIGN

For a UHF filter application, the transconductor must be able to closely approximate an ideal voltage-to-current converter at high frequencies, with minimal parasitic phase shifts. The use of small load capacitors is necessary; parasitic capacitors are typically a large proportion of the total capacitance and limit the lowest value of transconductance which can be used, since the time constant τ is equal to C/g_m. Increasing the total transconductance value can reduce the effect of parasitics, but also results in increased power consumption. The need to maintain low levels of noise and total harmonic distortion (THD) in order to achieve adequate dynamic range (DR) also needs to be considered in the

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transconductor design. Several high performance OTA architectures have been proposed. The folded-cascode, telescopic architecture [6] increases the output impedance and therefore provides high gain and good noise rejection. However, they are not suitable for high frequency linear phase filter design because the non-dominant pole degrades the performance of the filter [7]. A pseudo-differential topology is attractive for high power efficiency applications due to the absence of current sources. However, it suffers from low power supply rejection ratio (PSRR) [8]. For HDD applications, dynamic range need not be very high, typically 40dB is sufficient and the requirements on DC gain are also not stringent due the low Q of the linear phase design. In this design, a simple one-stage OTA based on a source degeneration topology and without internal nodes as shown in Figure 1 is utilized to meet these requirements for a UHF linear-phase filter.

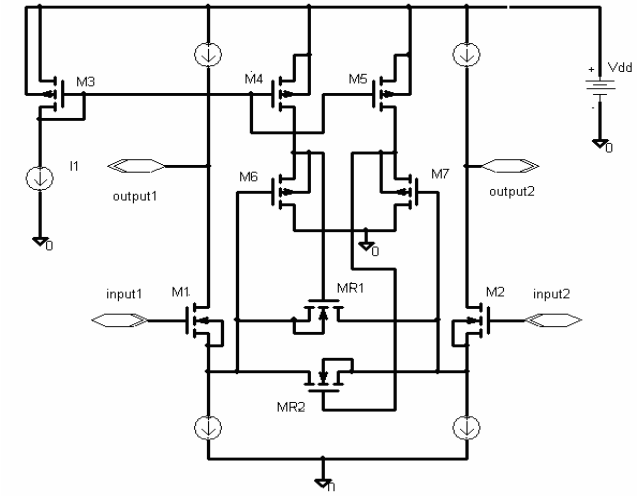

Figure1 OTA architecture

If the output resistance effects are ignored, the OTA output current with input voltage is:

$$i = g_{m1}\frac{v}{N+1}\sqrt{1-[\frac{v}{2V_{DSAT}(N+1)}]^2} \quad (1)$$

Therefore, the OTA low-frequency small signal transconductance is:

$$G_m = \frac{g_{m1}}{N+1} \quad (2)$$

where g_{m1} is matched with g_{m2} and is the low-electric-field transconductance of the differential pair M1, M2. N is the source degeneration factor. The two degenerated transistors M_{R1} and M_{R2} can be tuned by bias current I_1, in order to achieve different transconductance:

$$N \cong \frac{g_{m1}+g_{mb1}[1+\theta(V_{GS1}-V_{Tn})]}{\beta_{R1}(V_{GSR1}-V_{Tn})}+\theta(V_{GS1}-V_{Tn}) \quad (3)$$

Where $\theta\cdot(V_{GS1}-V_{Tn})$ accounts for the mobility degradation of the NMOS devices, and $g_{mb1,2}$ models the body effects. B is equal to $\mu_n C_{OX}(W/L)$. As shown in (3), increasing θ results in larger N. However, larger N leads to reduced G_m. While the source degeneration factor reduces the overall transconductance, the output impedance is boosted by the same factor. In fact, there is a cascode effect inherently present in the source degenerated topologies.

III. FILTER DESIGN

Selecting the correct transfer function for the filter is an important task. A critical design aspect of filters performing an equalization function in the HDD read channel is group delay variation, which should be less than about 5%, but does not necessarily have to be maximally flat. Both Bessel-Thomson and 0.05° Equiripple Linear phase approximations have been used to design equalizers for HDD applications. A 0.05° equiripple approximation of a linear phase response is more efficient than the Bessel family of filters.

On the other hand, the filter order is also important for UHF filter design. In HDD applications, both frequency response and phase response need to be considered. 4th, 5th, 7th and 8th order 0.05° equiripple linear phase filters have been designed [1-7]. However, none of these has a cut-off frequency greater than 600MHz. The design of UHF linear phase filter must optimize frequency performance, group delay ripple, power consumption, and chip area. Clearly, a lower order filter can reduce power consumption and chip area. However, the equiripple group delay response extends to higher frequencies with higher order filters about 2.5 times the cut-off frequency for the 7th order. Hence, a seventh-order linear phase lowpass filter based on a 0.05° equiripple approximation is considered in this paper.

Figure 2 shows a fully balanced realization of the seventh-order lowpass 0.05° equiripple linear phase filter using a current-mode LF structure. For equalization purposes, two additional gain-boost real zeros at the cut-off frequency are implemented using output summation OTAs g_{a5} and g_{a7}.

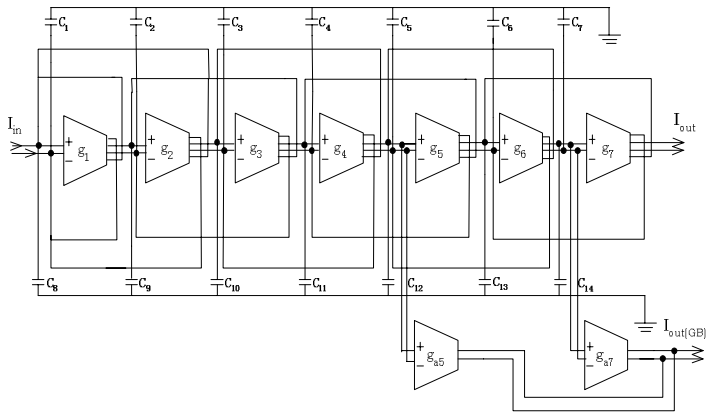

Figure 2 7th-order linear phase filter with gain boost structure

The normalized characteristic of the seventh–order 0.05° equiripple linear phase response, including the real zeros at the cut–off frequency, is given by:

$$H_d(s) = (s^2-1)/D(s) \quad (4)$$

Where

$$D(s) = 0.055617s^7 + 0.291094s^6 + 1.095656s^5 + 2.554179s^4 + 4.255922s^3 + 4.676709s^2 + 3.176156s + 1$$

The filter output with gain boost is taken from OTA g_{a7}. Note that the same filter response without gain boost is also available from the output of g_7. The overall transfer function of the circuit with gain boost can be derived as

$$H(s) = I_{out}/I_{in} = N(s)/D(s) \quad (5)$$

Where

$$N(s) = \alpha_5\tau_6\tau_7s^2 + (\alpha_5 + \alpha_7)$$

$$D(s) = \tau_1\tau_2\tau_3\tau_4\tau_5\tau_6\tau_7s^7 + \tau_2\tau_3\tau_4\tau_5\tau_6\tau_7s^6 + (\tau_1\tau_2\tau_3\tau_4\tau_5 + \tau_1\tau_2\tau_3\tau_4\tau_7 + \tau_1\tau_2\tau_3\tau_6\tau_7 + \tau_1\tau_2\tau_5\tau_6\tau_7 + \tau_1\tau_4\tau_5\tau_6\tau_7 + \tau_3\tau_4\tau_5\tau_6\tau_7)s^5 + (\tau_2\tau_3\tau_4\tau_5 + \tau_2\tau_3\tau_4\tau_7 + \tau_2\tau_3\tau_6\tau_7 + \tau_2\tau_5\tau_6\tau_7 + \tau_4\tau_5\tau_6\tau_7)s^4 + (\tau_1\tau_2\tau_3 + \tau_1\tau_2\tau_5 + \tau_1\tau_2\tau_7 + \tau_1\tau_4\tau_5 + \tau_1\tau_4\tau_7 + \tau_1\tau_6\tau_7 + \tau_3\tau_4\tau_5 + \tau_3\tau_4\tau_7 + \tau_3\tau_6\tau_7 + \tau_5\tau_6\tau_7)s^3 + (\tau_2\tau_3 + \tau_2\tau_5 + \tau_2\tau_7 + \tau_4\tau_5 + \tau_4\tau_7 + \tau_6\tau_7)s^2 + (\tau_1 + \tau_3 + \tau_5 + \tau_7)s + 1$$

The design formulae for the filter can be obtained by coefficient matching [9, 10]. The resulting pole and zero parameters are:

$$\tau_1=0.19106, \tau_2=0.47905, \tau_3=0.64409, \tau_4=0.74214, \tau_5=0.84224, \tau_6=1.00706, \tau_7=1.49877, \alpha_5=0.662536, \alpha_7=0.337464. \quad (6)$$

The filter is designed with identical unit OTAs using the CMOS OTA cell of Figure 1, with transconductance selected as 5.5mS. The cut-off frequency of the filter is designed for 650 MHz. Using the computed parameter values in (6), the capacitance values can be calculated, but the parasitic capacitance at the OTA input and output nodes must also be taken into account. After corrections for parasitic capacitance have been made, the actual capacitances are as listed below:

$C_1=C_8=0.2$pF, $C_2=C_9=0.7$pF, $C_3=C_{10}=1$pF, $C_4=C_{11}=1.2$pF, $C_5=C_{12}=1.3$pF, $C_6=C_{13}=1.6$pF, $C_7=C_{14}=2.5$pF.

IV. SIMULATION RESULTS

The OTAs and filter were designed and simulated using BSIM 3v3 Spice models for a TSMC 0.18μm CMOS process [11]. The simulated DC transfer function and small-signal AC response for the OTA are shown in Figures 3 and 4, respectively.

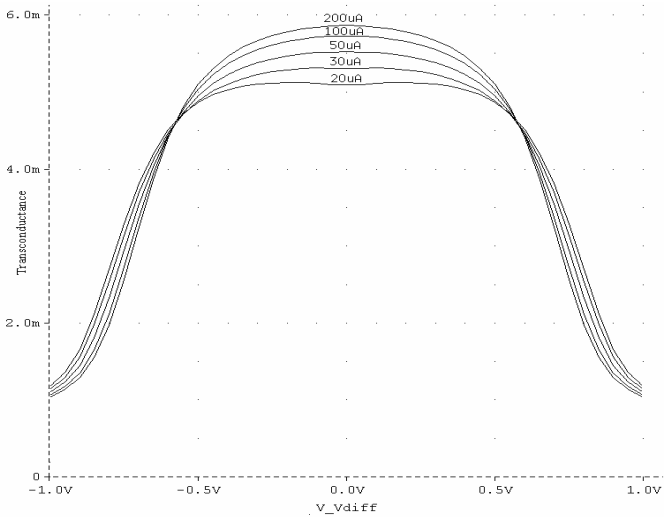

Figure3 Simulated DC responses of OTA with different bias currents

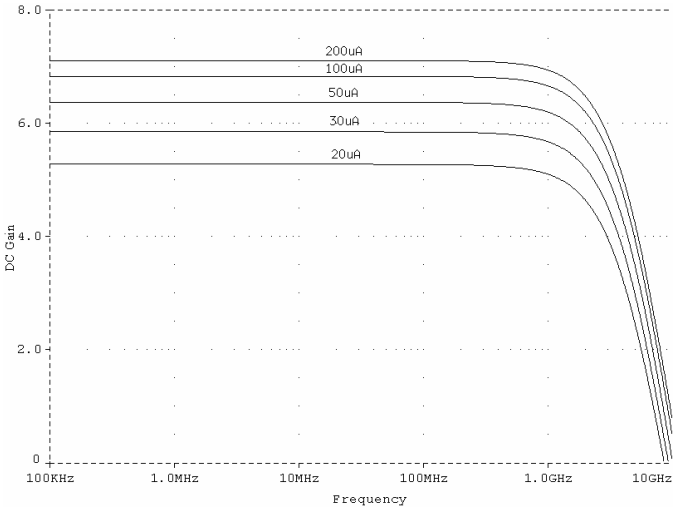

Figure 4 Simulated AC reposes of OTA with different bias currents

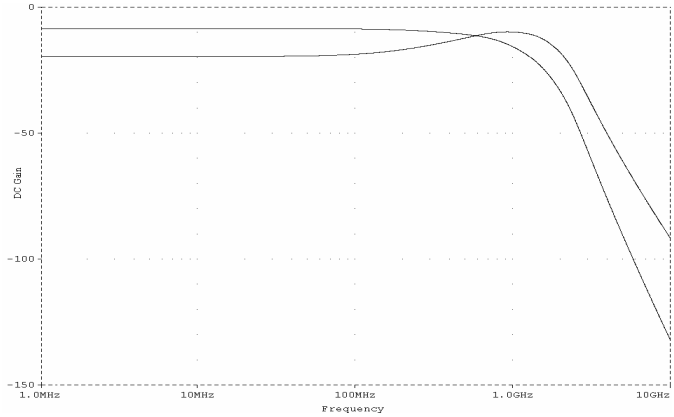

Figure 5 Magnitude response of proposed filter

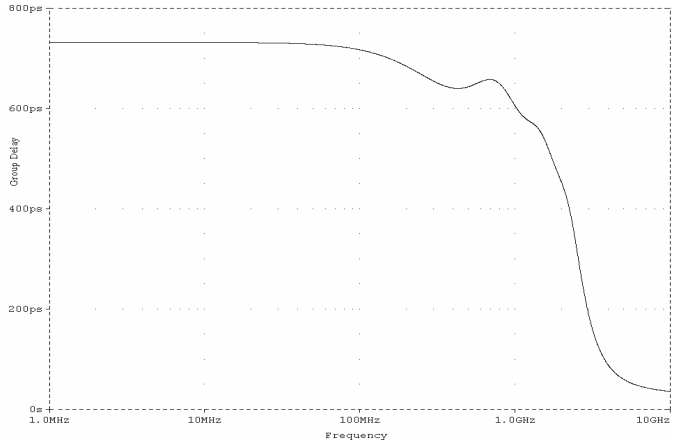

Figure 6 Group delay response of proposed filter

Figure 5 shows the magnitude response of the filter with and without gain boost. As can be seen, the gain boost of the filter is 5dB at the cut-off frequency. By varying the bias current I_1 of the unit OTA cell, the tuning range of cut-off frequency without gain boost is 590-690MHz. The total power consumption of the filter is 370mW. The dynamic range is 48dB with 1% THD at f_c=650MHz. The filter phase response is fairly linear, as can be seen from Figure 6. The group delay ripple of filter for $f_c/5 \leq f \leq 1.4\, f_c$ is approximately 5% over the whole tuning range. This is well within the limit of the read channel filter specification. A performance comparison of the proposed filter with other designs in the literature is given in Table 1.

V. CONLUSIONS

A CMOS 650MHz current–mode seventh–order linear phase leap–frog filter with 5dB gain boost has been described. A linear OTA using a source degeneration topology with a typically large transconductance has been used. Simulation results using models for a 2.5V 0.18µm CMOS process yield a cut-off frequency tuning range of 590-690MHz, dynamic range of 48dB, and group delay ripple of 4.5%. This UHF current–mode LF filter is therefore well suited to hard disk read channel applications.

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Table I The comparison with other linear phase lowpass filter

Parameters	**Specifications**				
Reference	[1]	[2]	[4]	[5]	This work
Filter_Conf.	Cascade	Cascade	VM LF	VM LF	CM LF
Range MHz	30-120	550	50-150	100	590-690
GDR	3%	4%	4.50%	7%	4.5%
DR	45dB	50dB	65dB	55dB	48dB
PC mW	120	140	216	322	370
P. Supply	2.5V	3.3V	2.5V	5V	2.5V
CMOS Tech.	0.25um	0.35um	0.25um	0.25um	0.18um

GDR = group delay ripple; DR = dynamic range; PC = power consumption
VM = voltage–mode; CM = current–mode